Date : Mar. 26, 2013

TECHNICAL DATA	
Product Name	**TX76D02VM0BAA**

(NOTES)

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Japan Display Inc.

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RECORD OF REVISIONS

Date	Sheet No.	Summary

Note : The LED for the backlight unit is integrated within this module.

Product Name : TX76D02VM0BAA

Effective Display Area	: (H)641.28 × (V)404.808	(mm)
Number of Pixels	: (H)2,560 × (V)1,616	(pixels)
Aspect ratio	: 16 : 10.1	
Pixel Pitch	: (H)0.2505 × (V)0.2505	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Frame frequency	: 60 Hz	
Top Polarizer Type	: Anti-glare (Surface hardness: 2H)	
Number of Colors	:1,073,741,824 colors (10bit)	
LCM Mode	: IPS-Pro (New Process)	
Input Signal	: 4-channel LVDS (LVDS = Low Voltage Differential Signaling)	
Back Light	: Edge Light Type with white LED	
External Dimensions	: (H)687.3 × (V)454.4 × (t)37.5 (mm)	
Weight	: 7100g typ	
RoHS	: Compliance	

1. ABSOLUTE MAXIMUM RATINGS

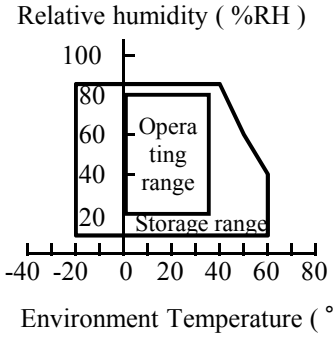
1.1 ENVIRONMENT ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Panel surface Temperature	0	50	-20	60	°C	1)
Humidity	2)		2)		%RH	1)
Vibration	-	2.45 (0.25G)	-	9.8 (1.0G)	m/s^2	3), 5)
Shock	-	14.7 (1.5G)	-	294 (30G)	m/s^2	4), 5)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	
TCON Surface Temperature	-	85	-	85	°C	6)
LED Driver Parts Temperature	-	85	-	85	°C	7)
Rear frame Temperature	-	65	-	65	°C	8)

Notes

1) Temperature and Humidity should be applied to the panel surface of the TFT module and not to the system installed with the module.

2) Ta ≤ 40°C : Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta > 40°C : Relative humidity should be lower than the moisture of the 85%RH at 40°C .



3) Frequency of vibration is between 15Hz and 100Hz, except resonance point and z-direction (panel face top and bottom).

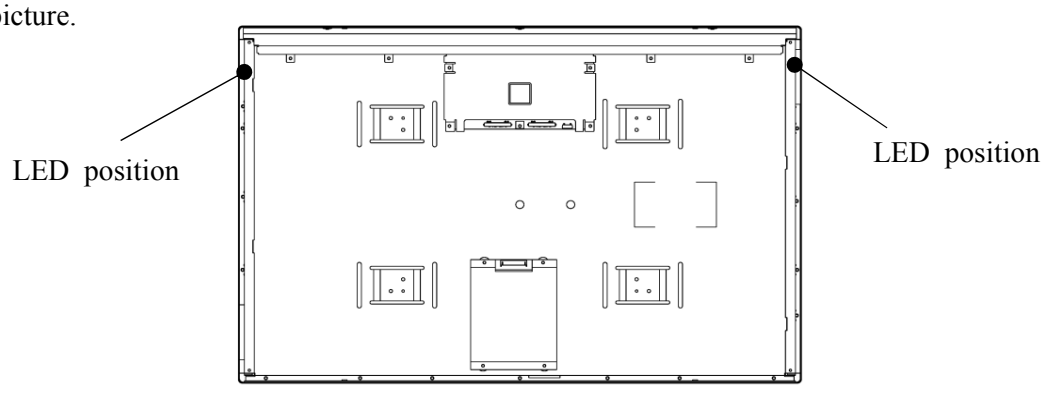
4) Pulse width of the shock wave pattern is 10ms approximately.

5) The LCD module should be mounted and fixed to a monitor chassis by all 16 screws whose holes are located two each at top, bottom, right and left side, and remaining 8 pcs at rear side of the module.

6) FPGA-IC

7) MOSFET

8) See below picture.



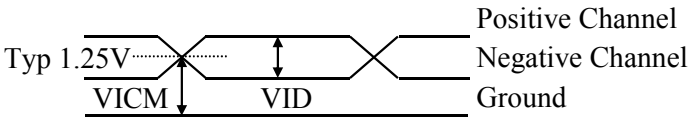
1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT-LCD Module

Vss = 0 V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	-	13.2	V	
Input Differential voltage swing	V_{ID}	100	900	mV	1)
Input common mode voltage	V_{ICM}	500	1800	mV	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Notes 1) It is applied to LVDS specifications.



2) Discharge Coefficient: 200pF-250Ω, Environmental: 25°C-70%RH

3) It is applied to I/F connector pins.

4) It is applied to the surface of a metallic bezel and a LCD panel.

(2) LED driver

Vss = 0 V

Item	Symbol	Min.	Max.	Unit	Note
Input Voltage	Vin	-	30.0	V	
ON/OFF Control Input Voltage	ON/OFF	0	6.0	V	
PWM dimming signal Voltage	PWM	0	6.0	V	

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent environment. All initial optical characteristic items should be applied when panels have been shipped.

Measuring equipment : CS-1000A or CA-210, EZ-contrast

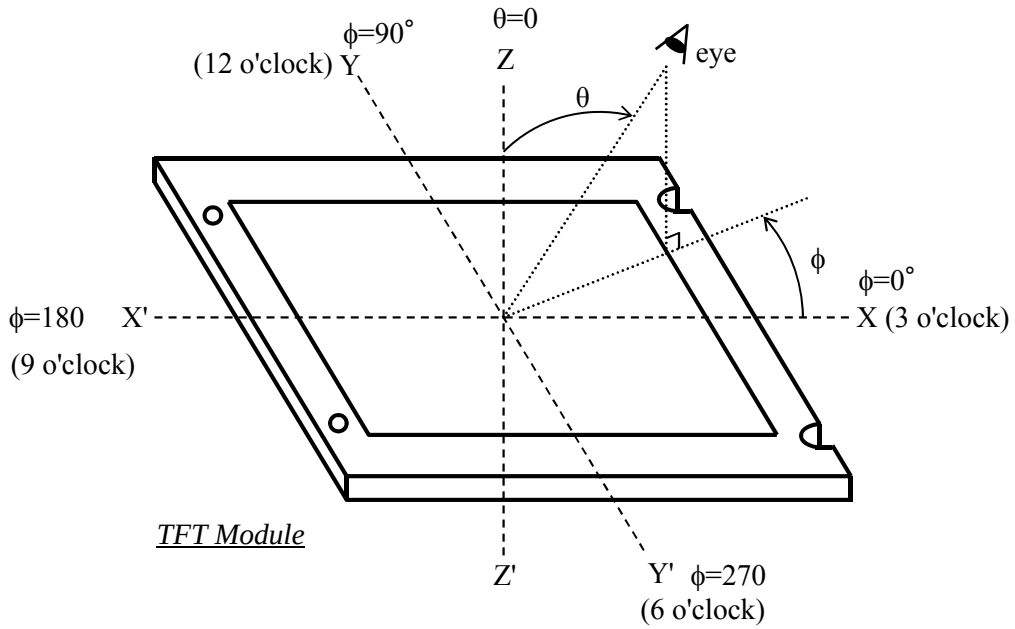
Ambient Temperature =25±3°C, VDD=12.0V, fV=60Hz, Vin=24V

2.1 SPECIFICATION

Items			Condition	Min.	Typ.	Max.	Unit	Notes
Contrast ratio			θ = 0	(900)	(1100)	-	-	1), 2)
Contrast ratio at ±85°			ϕ = 0, 90, 180, 270	(50)	-	-	°	1)
Brightness			θ = 0	(550)	(650)	-	cd/m^2	6)
Brightness uniformity	Gray scale = 1023		θ = 0	(70)	-	-	%	4)
	Gray scale = 511			(65)	-	-		
Color chromaticity	Red	x	θ = 0	(0.615)	(0.645)	(0.675)	ΔCIE	1)
		y		(0.297)	(0.327)	(0.357)		
	Green	x		(0.278)	(0.308)	(0.338)		
		y		(0.590)	(0.620)	(0.650)		
	Blue	x		(0.116)	(0.146)	(0.176)		
		y		(0.033)	(0.063)	(0.093)		
	White	x		(0.269)	(0.299)	(0.329)		
		y		(0.285)	(0.315)	(0.345)		
Variation of color point by viewing angle (Gray scale = 1023)			θ = ±80 ϕ = 0, 90, 180, 270	-	-	(0.04)	Δu'v'	5)
Response time	Tr		θ = 0	-	(10)	(20)	ms	3)
	Tf			-	(10)	(20)		
	Total			-	(20)	(40)		
γ			θ = 0	-	(2.2)	-	-	

Notes

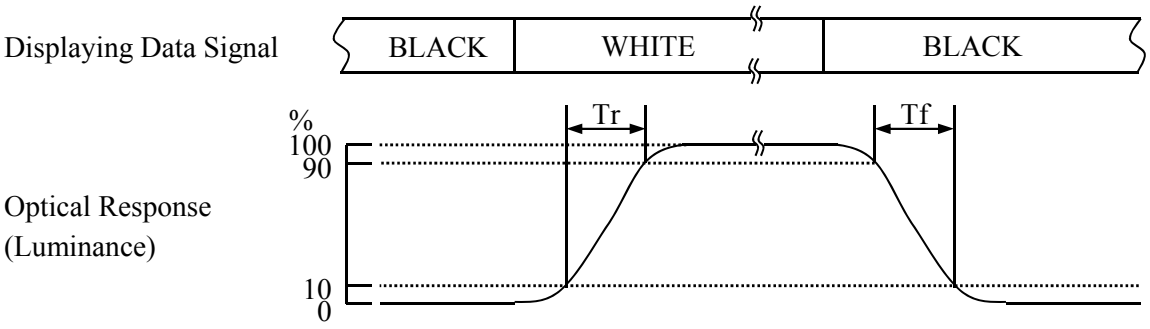
1) Definition of Viewing Angle (gray scale = 1023)



2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance whilst displaying WHITE)}}{\text{(Luminance whilst displaying BLACK)}}$$

3) Definition of Response Time



Panel surface temperature = 45°C

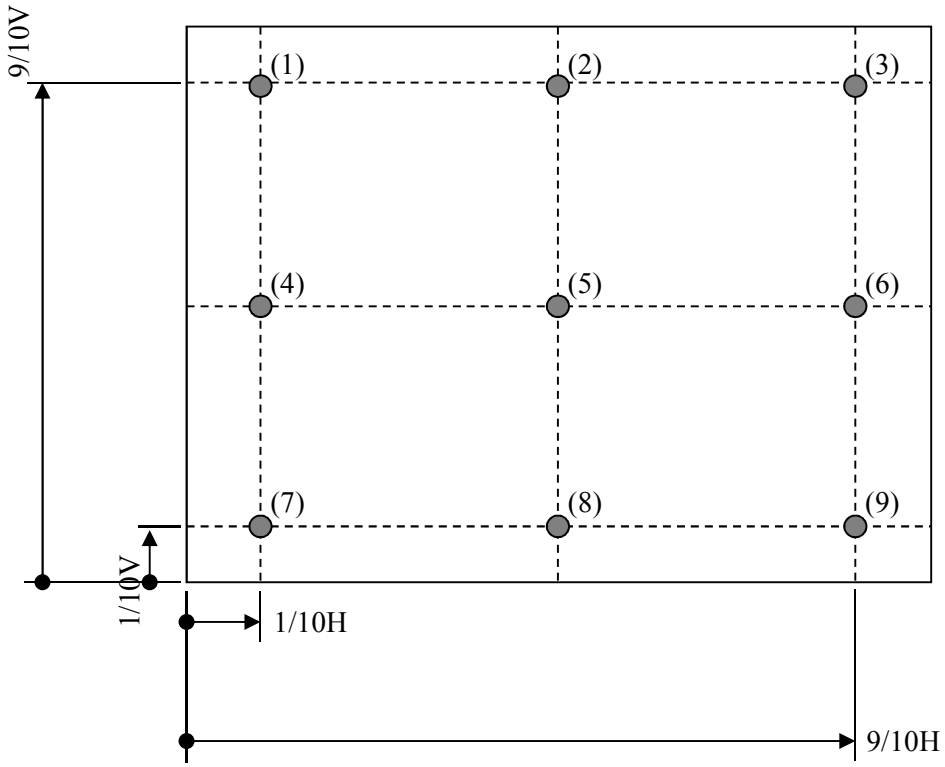
4) Definition of Brightness Uniformity

Display pattern is white (511/1023 level). The brightness uniformity is defined by the following equation. Brightness at each point is measured and then Buni can be calculated using the maximum and minimum brightness values.

$$Buni = \left(\frac{Bmin}{Bmax}\right) \times 100$$

where, Bmax = Maximum brightness measured.

Bmin = Minimum brightness measured.



: measuring point

5) Variation of color position on CIE is defined as difference between colors for TFT-LCD module.

$$u' = \frac{4x}{-2x + 12y + 3} \qquad v' = \frac{9y}{-2x + 12y + 3}$$

6) PWM dimming signal should be 100%.

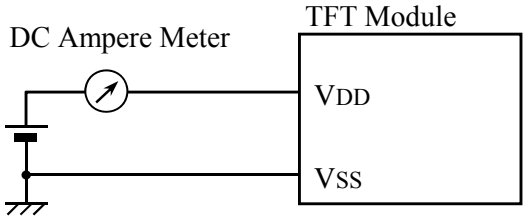
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD MODULE

Ta=25°C, Vss=0V

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	11.4	12.0	12.6	V	
Power Supply Current	IDD	-	1.4	1.8	A	1),2)
Ripple Voltage of Power Supply	VDDR	-	-	0.15	V	

Notes 1) DC current at fv=60.0Hz, fCLK=67.5MHz, VDD=12.0V and display pattern is a full White (1023).



2) A protection fuse is built into this module. Current capacity of the power supply for VDD should be greater than 6A, so that the fuse can 'blow' if there is a problem with the power supply.

3.2 BACK LIGHT

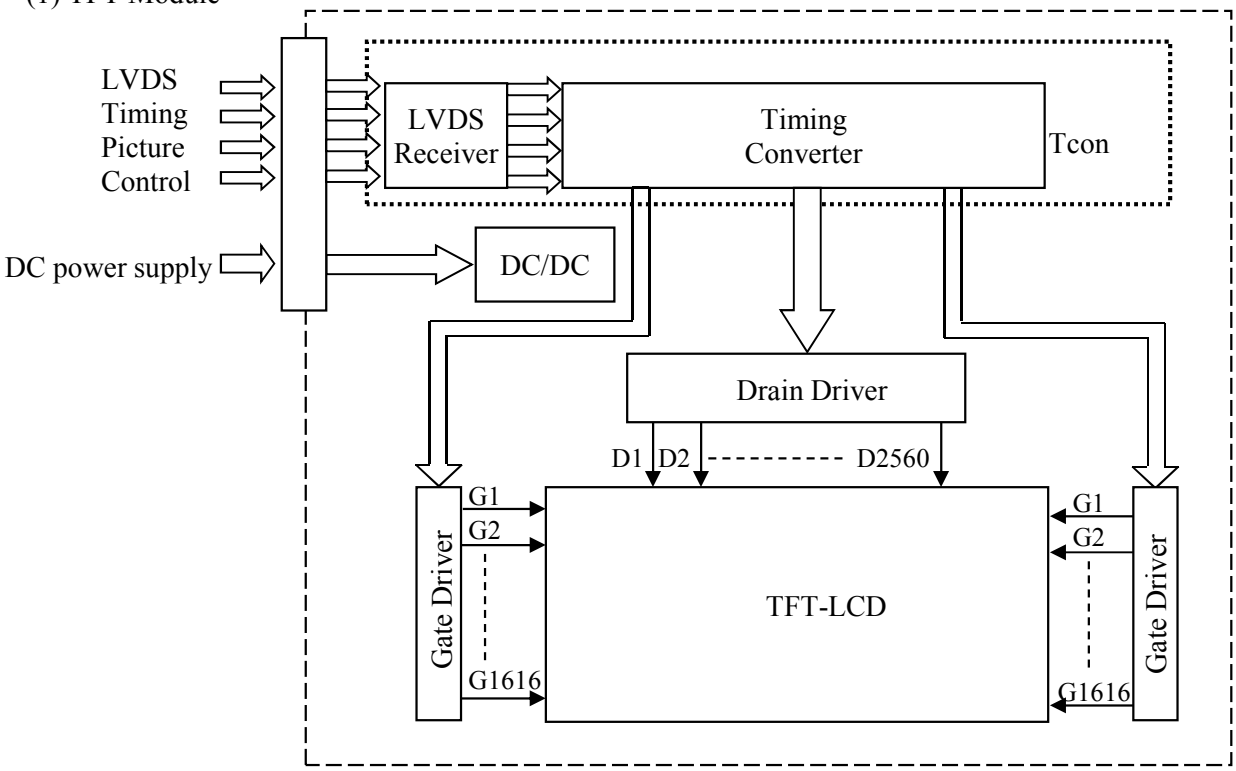
Ta=25°C

Item		Symbol		Value			Unit	Note
				Min	Typ	Max		
Input Voltage		Vin		21.6	24	26.4	V	
Input Current		Iin		-	3.8	4.2	A	
Input Power		Pin		-	91.2	111	W	
ON/OFF Control Input Voltage	ON	ON/OFF		2.5	3.3	5.0	V	
	OFF			0	-	0.5	V	
PWM dimming signal Input Voltage		PWN	High	2.5	3.3	5.0	Vdc	
			LOW	0	-	0.9	Vdc	
PWM Duty		-		10	-	100	%	
PWM Frequency		PWMf		(140)	(150)	(160)	Hz	1)

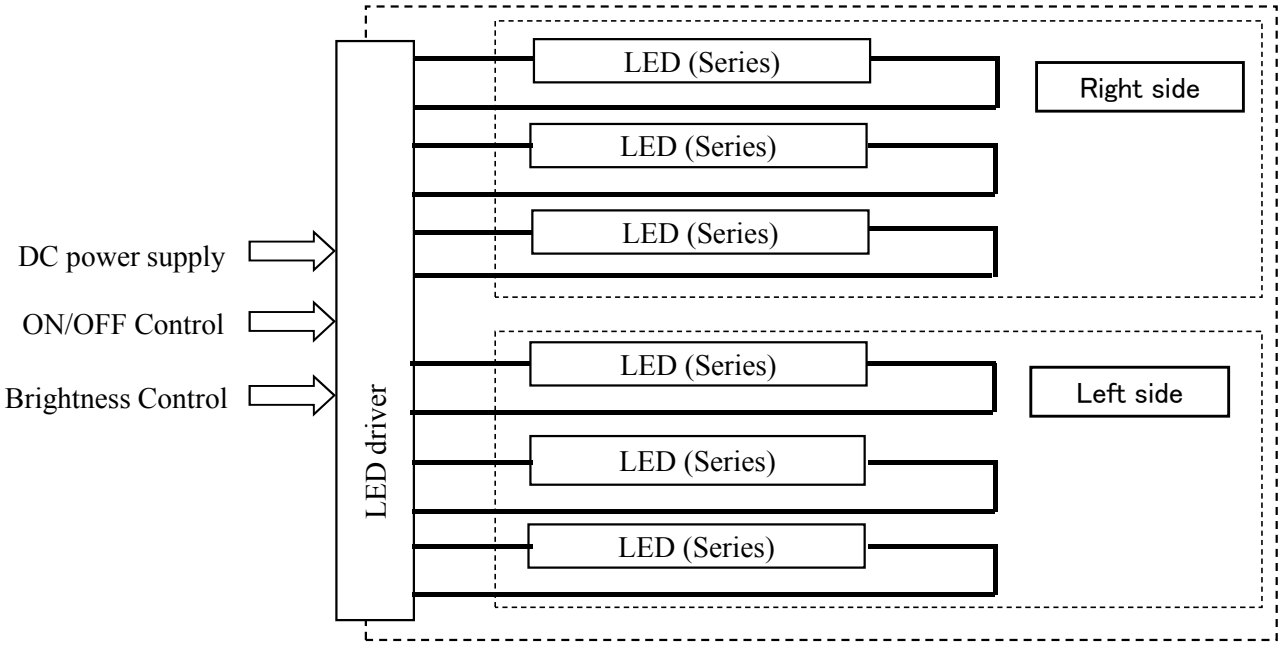
1) specifications should be applied at 140Hz～160Hz.

4. BLOCK DIAGRAM

(1) TFT Module



(2) Back light unit



5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD MODULE INPUT CONNECTOR : HIROSE

Plug FX15S-41S-0.5SH (PCB connector side)

FX15S-41P-C (cable side)

LEFT I/F connector (CN1) (CH1, 2)

Power Supply	1	VDD
	2	VDD
	3	VDD
	4	VDD
	5	VDD
	6	VSS
	7	VSS
	8	VSS
	9	VSS
CH1	10	ARX0n
	11	ARX0p
	12	ARX1n
	13	ARX1p
	14	VSS
	15	ARX2n
	16	ARX2p
	17	ACLKn
	18	ACLKp
	19	VSS
	20	ARX3n
	21	ARX3p
	22	ARX4n
	23	ARX4p
	24	VSS
CH2	25	BRX0n
	26	BRX0p
	27	BRX1n
	28	BRX1p
	29	VSS
	30	BRX2n
	31	BRX2p
	32	BCLKn
	33	BCLKp
	34	VSS
	35	BRX3n
	36	BRX3p
	37	BRX4n
	38	BRX4p
	39	VSS
	40	TEST
	41	TEST

RIGHT I/F connector (CN2) (CH3, 4)

Power Supply	1	VDD
	2	VDD
	3	VDD
	4	VDD
	5	VDD
	6	VSS
	7	VSS
	8	VSS
	9	VSS
CH3	10	CRX0n
	11	CRX0p
	12	CRX1n
	13	CRX1p
	14	VSS
	15	CRX2n
	16	CRX2p
	17	CCLKn
	18	CCLKp
	19	VSS
	20	CRX3n
	21	CRX3p
	22	CRX4n
	23	CRX4p
	24	VSS
CH4	25	DRX0n
	26	DRX0p
	27	DRX1n
	28	DRX1p
	29	VSS
	30	DRX2n
	31	DRX2p
	32	DCLKn
	33	DCLKp
	34	VSS
	35	DRX3n
	36	DRX3p
	37	DRX4n
	38	DRX4p
	39	VSS
	40	TEST
	41	TEST

Notes 1) All VSS pins should be grounded.

2) All VDD pins should be connected to +12.0 V (typ.).

3) TEST Pins are only for Hitachi use.

5.2 BACK-LIGHT UNIT

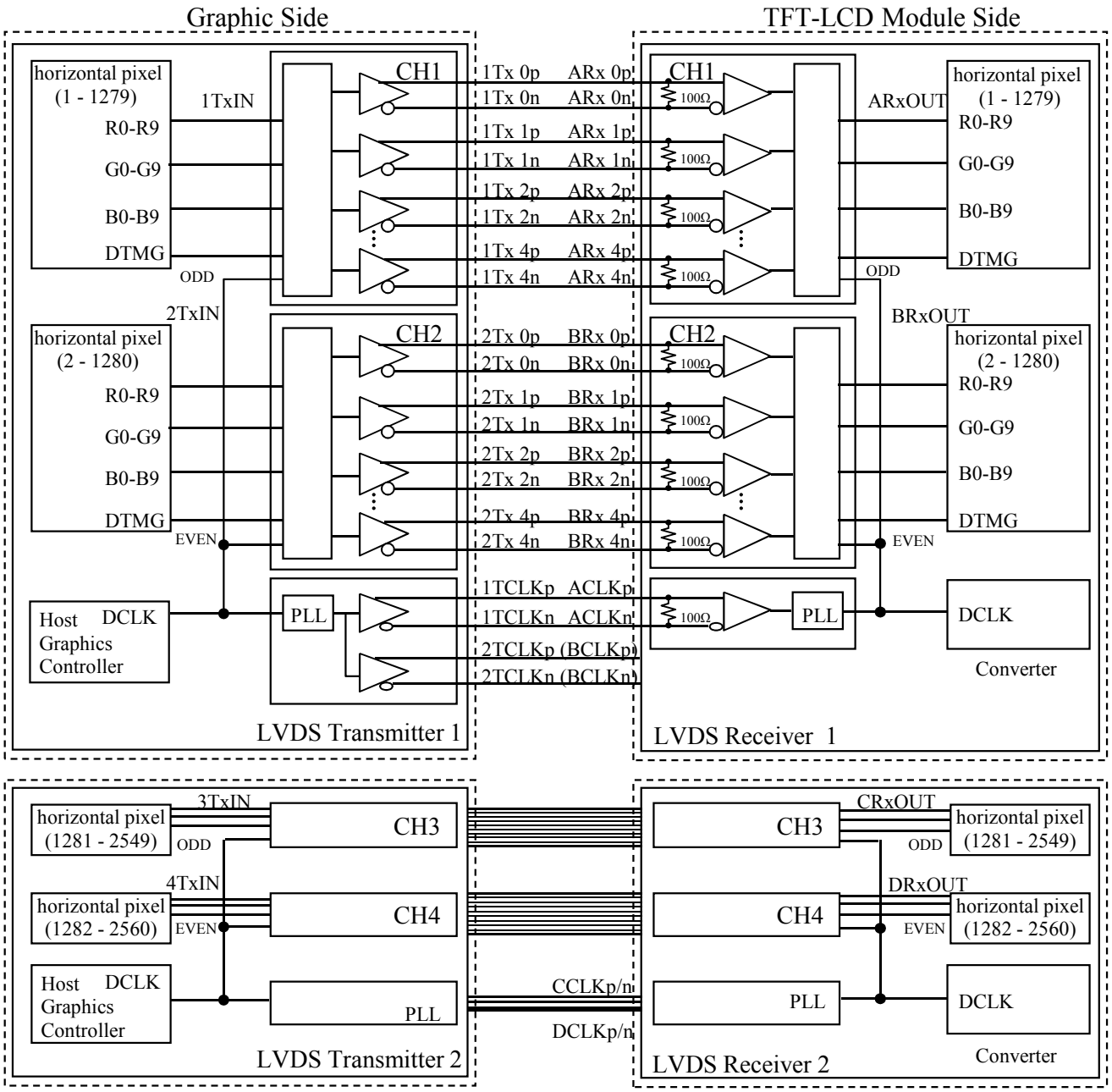
CN3 : JST S14B-PH-SM4-TB (Inverter PCB Connector side)
(Matching connector : JST PHR-14 (Cable side))

Pin No.	Symbol	Description	Note
1	VIN	Power Supply (typ. 24.0V)	1)
2	VIN		
3	VIN		
4	VIN		
5	VIN		
6	VSS	GND (0V)	2)
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	NC	Not Connecting	
12	ON/OFF	High : Lamp ON, Low : Lamp OFF	3)
13	NC	Not Connecting	
14	PWM	PWM dimming signal	4)

Notes

1) All VIN pins should be connected to +24.0V (Typ.).
2) All VSS pins should be grounded. The metal bezel is internally connected to GND.
3) High level : 2.5 ~ 5.0V, Low level : 0 ~ 0.5V
4) High level : 2.5 ~ 5.0V, Low level : 0 ~ 0.9V

5.3 BLOCK DIAGRAM OF INTERFACE

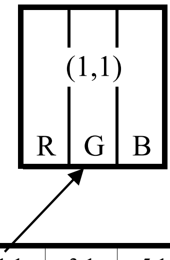


R0 ~ R9 : Pixel R Data
G0 ~ G9 : Pixel G Data
B0 ~ B9 : Pixel B Data
DTMG : Display timing signal
DCLK : Dot Clock (DCLK of CH2, 4 are not used.)

Notes 1) The host system must have the transmitter in-situ to drive the module.
2) LVDS cable impedance should be 100 ohms per twisted-pair line when used differentially.

5.4 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent pixel is latched during one cycle of DCLK.



pixel : R0 ~ R9 : R data
G0 ~ G9 : G data
B0 ~ B9 : B data

1,1	3,1	5,1	…	1279,1	2,1	4,1	6,1	…	1280,1	1281,1	1283,1	1285,1	…	2549,1	1282,1	1284,1	1286,1	…	2560,1
1,2	3,2	5,2	…	1279,2	2,2	4,2	6,2	…	1280,2	1281,2	1283,2	1285,2	…	2549,2	1282,2	1284,2	1286,2	…	2560,2
1,3	3,3	5,3	…	1279,3	2,3	4,3	6,3	…	1280,3	1281,3	1283,3	1285,3	…	2549,3	1282,3	1284,3	1286,3	…	2560,3
1,4	3,4	5,4	…	1279,4	2,4	4,4	6,4	…	1280,4	1281,4	1283,4	1285,4	…	2549,4	1282,4	1284,4	1286,4	…	2560,4
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1,1616	3,1616	5,1616	…	1279,1616	2,1616	4,1616	6,1616	…	1280,1616	1281,1616	1283,1616	1285,1616	…	2549,1616	1282,1616	1284,1616	1286,1616	…	2560,1616

CH1 (LEFT_ODD) CH2 (LEFT_EVEN) CH3 (RIGHT_ODD) CH4 (RIGHT_EVEN)

5.5 RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color \ Input		Red Data								Green Data								Blue Data							
		R9	R8	R7	···	R3	R2	R1	R0	G9	G8	G7	···	G3	G2	G1	G0	B9	B8	B7	···	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1022)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green (1022)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale :

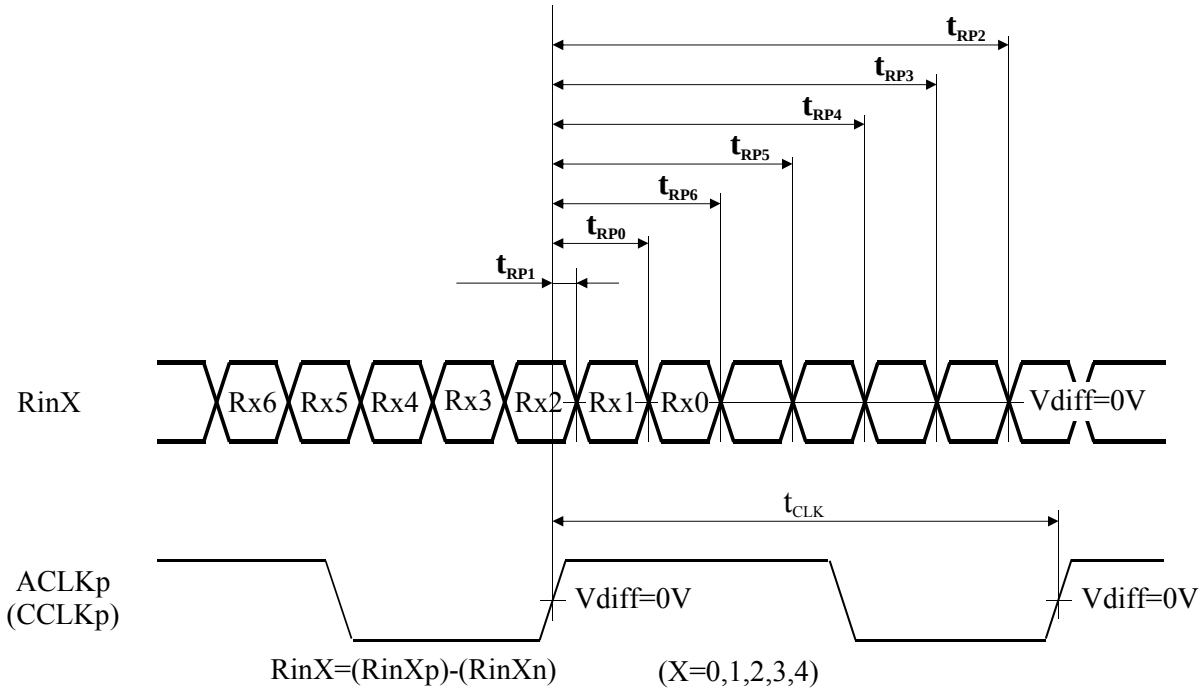
Color (n) : Number in parenthesis indicates gray scale level. Larger n corresponds to a brighter level.

2) Data : 1 : High, 0 : Low

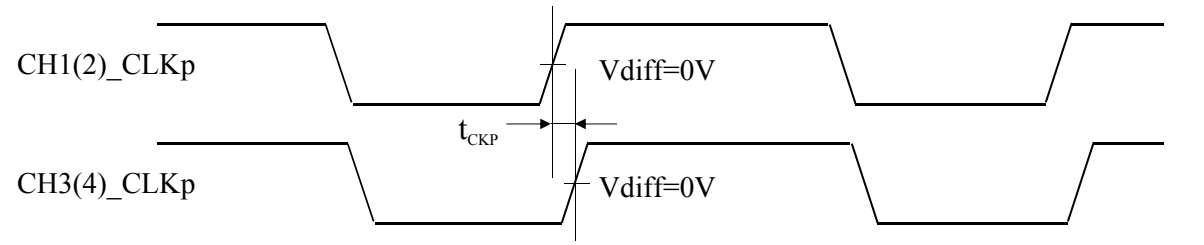
6. INTERFACE TIMING

6.1 LVDS RECEIVER TIMING CHARACTERISTICS

(Regulation with the Input Terminal of the Module)

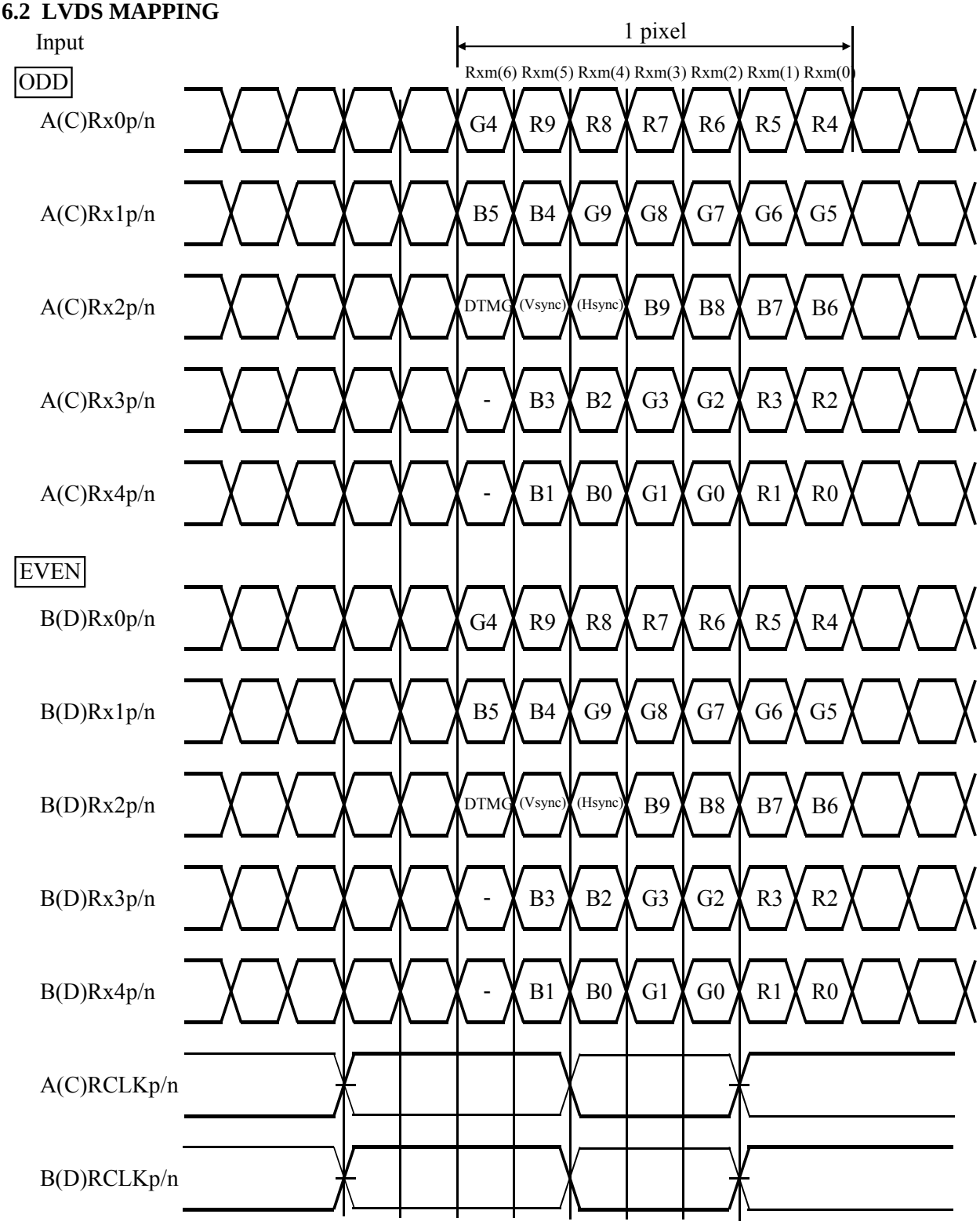


Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
DCLK	Parameter	$1/t_{CLK}$	66.5	67.5	68.5	MHz	
t_{sk}	Data Skew Margin	-	-450	0	+450	ps	
RinX (X=0,1,2, 3,4)	Input Data Position0	t_{RP0}	$\frac{1}{7}t_{CLK}{}^{-tsk}$	$\frac{1}{7}t_{CLK}$	$\frac{1}{7}t_{CLK}{}^{+tsk}$	ns	
	Input Data Position1	t_{RP1}	0^{-tsk}	0	0^{+tsk}		
	Input Data Position2	t_{RP2}	$\frac{6}{7}t_{CLK}{}^{-tsk}$	$\frac{6}{7}t_{CLK}$	$\frac{6}{7}t_{CLK}{}^{+tsk}$		
	Input Data Position3	t_{RP3}	$\frac{5}{7}t_{CLK}{}^{-tsk}$	$\frac{5}{7}t_{CLK}$	$\frac{5}{7}t_{CLK}{}^{+tsk}$		
	Input Data Position4	t_{RP4}	$\frac{4}{7}t_{CLK}{}^{-tsk}$	$\frac{4}{7}t_{CLK}$	$\frac{4}{7}t_{CLK}{}^{+tsk}$		
	Input Data Position5	t_{RP5}	$\frac{3}{7}t_{CLK}{}^{-tsk}$	$\frac{3}{7}t_{CLK}$	$\frac{3}{7}t_{CLK}{}^{+tsk}$		
	Input Data Position6	t_{RP6}	$\frac{2}{7}t_{CLK}{}^{-tsk}$	$\frac{2}{7}t_{CLK}$	$\frac{2}{7}t_{CLK}{}^{+tsk}$		



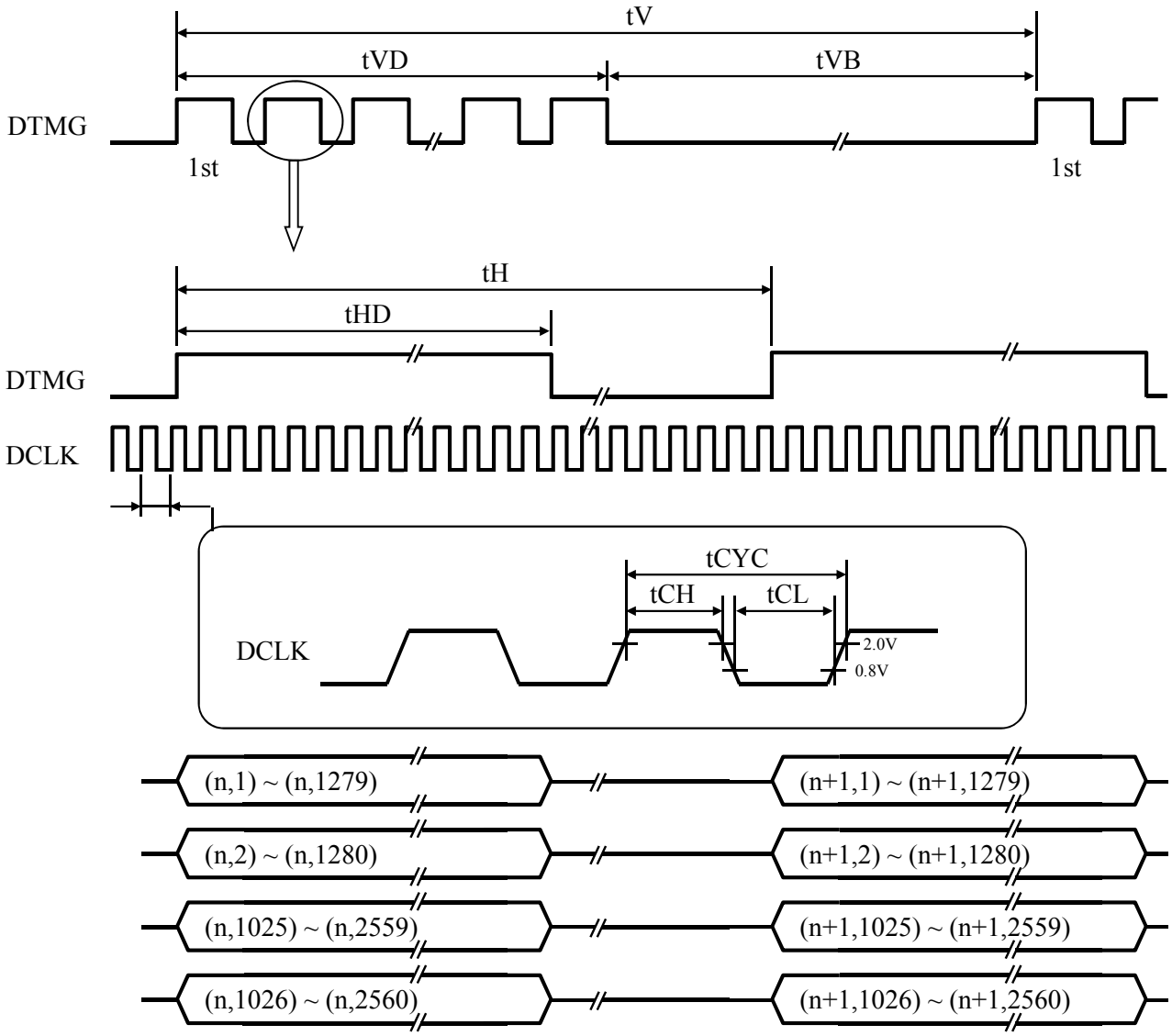
Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLKp	Input CLK Position	t_{CKP}	-1	0	+1	DCLK	

6.2 LVDS MAPPING



R0 ~ R9 : Pixel R Data (9;MSB, 0;LSB)
G0 ~ G9 : Pixel G Data (9;MSB, 0;LSB)
B0 ~ B9 : Pixel B Data (9;MSB, 0;LSB)
DTMG : Display timing signal
RCLK : Dot Clock

6.3 TIMING CHART



(n=1,2,3, ~ 1615)

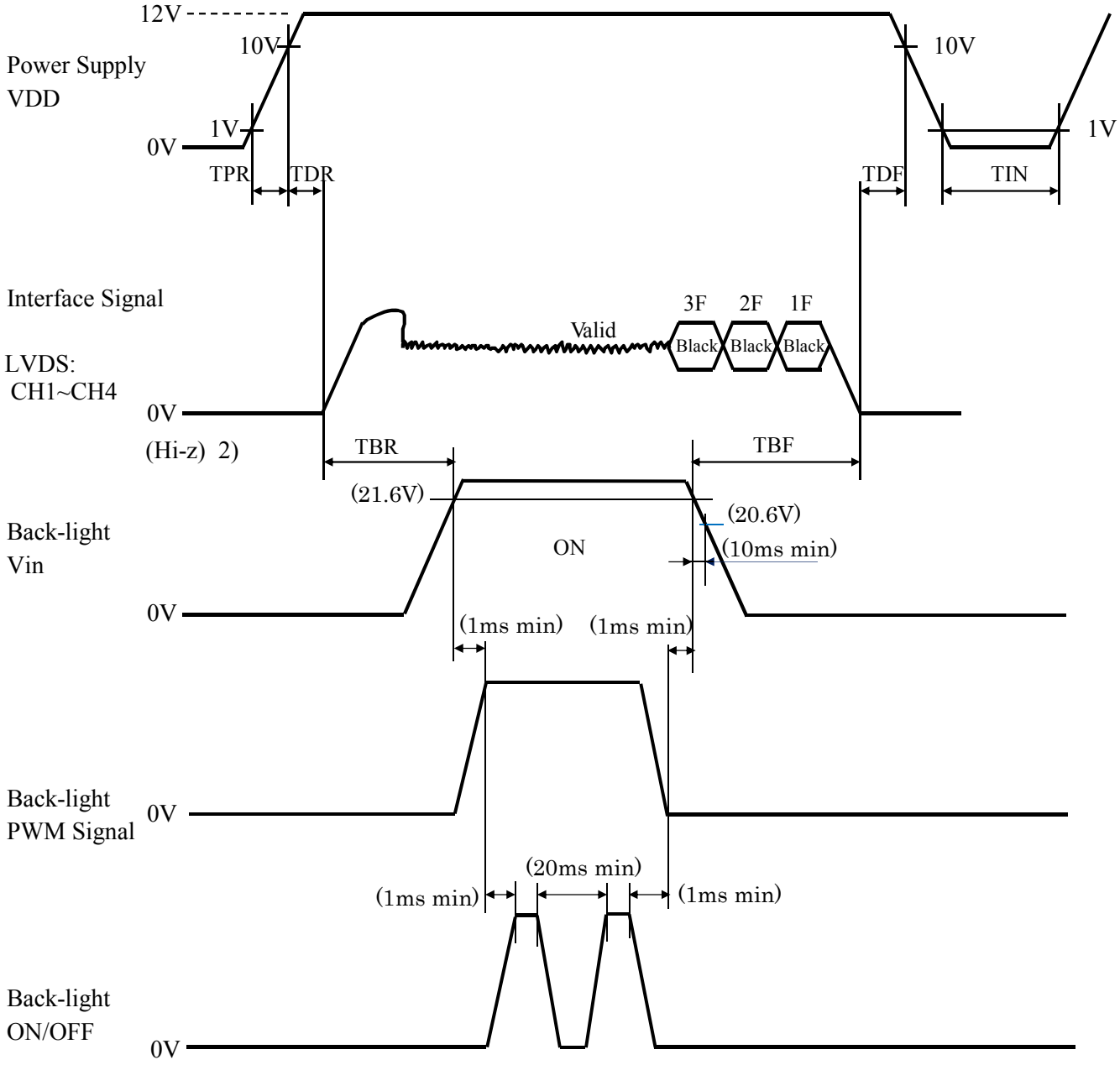
6.4 INTERFACE TIMING SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/tCYC	66.5	67.5	68.5	MHz	1)
	Duty	tCH/tCYC	45	50	55	%	
DTMG	Period (Hor)	tH	664	690	840	tCK	
	Width Active (Hor)	tHD	640	640	640	tCK	
	Period (Ver)	tV	1620	1630	1730	tH	
	Width Active (Ver)	tVD	1616	1616	1616	tH	
	DTMG Jitter	ΔtVB	-1	0	1	tH	

Note

1) Since DCLK and inverter driving frequency are optimized, please be noted that DCLK should be set within this spec. Otherwise, optical side effect may happen.

6.5 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Notes

1) Timing of the power supply voltage and input signals should be set using the following specifications.

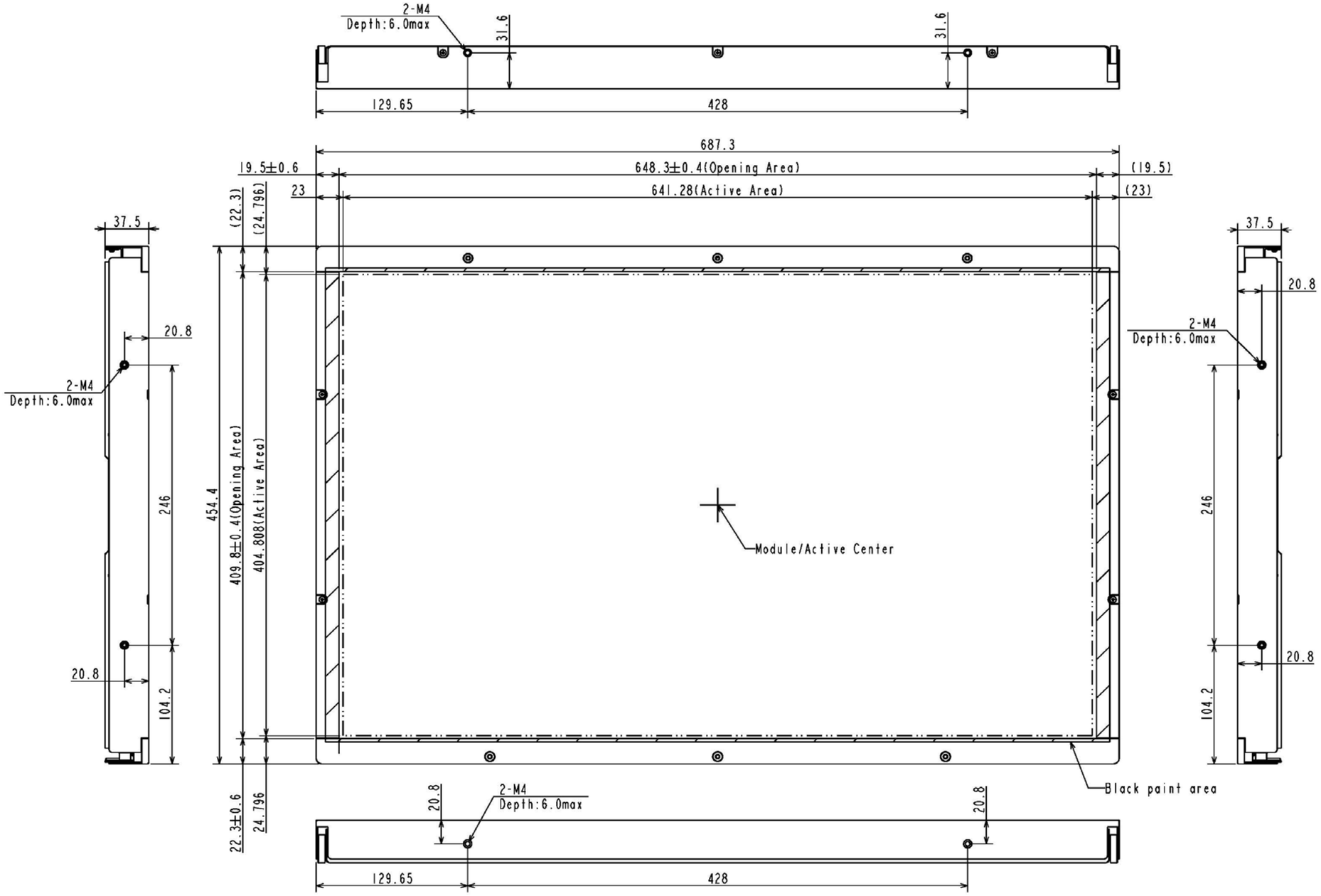
0.5ms ≤ TPR ≤ 10ms
10ms ≤ TDR ≤ 50ms
-10ms ≤ TDF ≤ 50ms
TIN ≥ 1s
TBR ≥ 500ms
TBF ≥ 100ms

*Before the end of the Interface Signal, black image is shown for the last 3 frames. Refer to above Interface Signal Timing.

2) LVDS signals must be Low or High-impedance (Hi-z) state when VDD is off.

7. DIMENSIONAL OUTLINE

(1) Front View



Note 1) The dimension in a parenthesis is reference value.
2) Unspecified tolerance to be ± 1.0mm.
3) Maxmum torque for M4 screw : 1.2N・m.

Unit : mm
Scale : NTS

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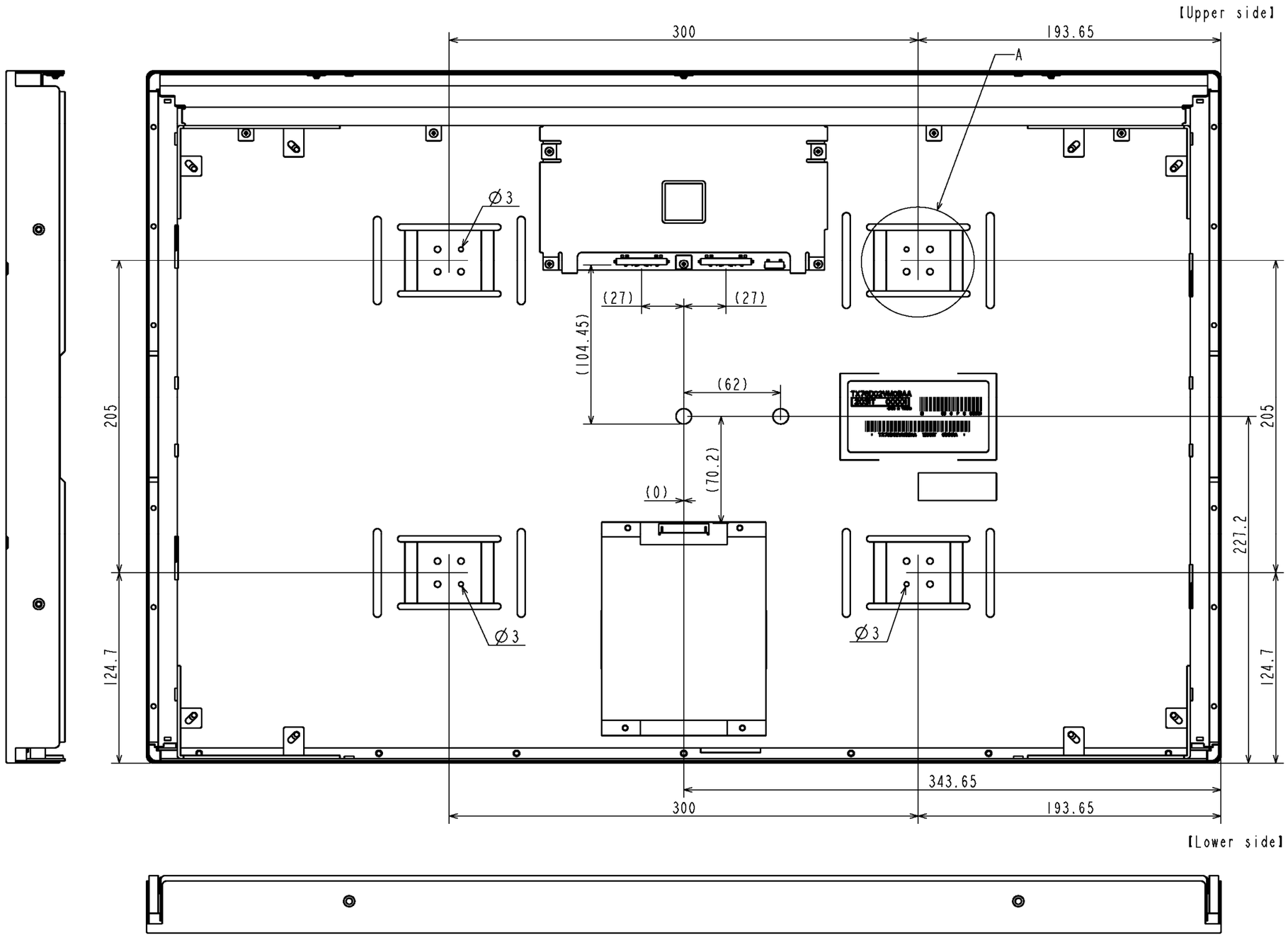
(2) Rear View



Note 1) The dimension in a parenthesis is reference value.
2) Unspecified tolerance to be ± 1.0mm.
3) Maxmum torque for M4 screw : 1.2N・m.

Unit : mm
Scale : NTS

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